VHDL Style Observations

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Counter Design – Version 1

```
entity dec_counter is
    Port ( mclk : in  STD_LOGIC;
           en : in  STD_LOGIC;
           ce_out : out  STD_LOGIC);
end dec_counter;

architecture Behavioral of dec_counter is
   signal r_reg: unsigned(3 downto 0);
   signal r_next: unsigned(3 downto 0);
begin
   process(mclk,en,r_reg)
   begin
      if (mclk'event and mclk='1') then
         if (en = '1') then
            if (r_reg = "1001") then
               r_reg <= "0000";
               ce_out <= '1';
            else
               r_reg <= r_next;
               ce_out <= '0';
            end if;
         end if;
      end if;
   end process;
   r_next <= r_reg + 1;
end Behavioral;
```

Version 1 – FPGA Utilization

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	5	4,896	1%	
Number of 4 input LUTs	5	4,896	1%	
Number of occupied Slices	3	2,448	1%	
Number of Slices containing only related logic	3	3	100%	
Number of Slices containing unrelated logic	0	3	0%	
Total Number of 4 input LUTs	5	4,896	1%	
Number of bonded IOBs	3	66	4%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.25			

Version Comparisons

Version 1

```
architecture Behavioral of dec_counter is
   signal r_reg: unsigned(3 downto 0);
   signal r_next: unsigned(3 downto 0);
begin
   process(mclk,en,r_reg)
   begin
      if (mclk'event and mclk='1') then
         if (en = '1') then
            if (r_reg = "1001") then
               r_reg <= "0000";
               ce_out <= '1';
            else
               r_reg <= r_next;
               ce_out <= '0';
            end if;
         end if;
      end if;
   end process;
   r_next <= r_reg + 1;
end Behavioral;
```

Version 2

```
architecture Behavioral of dec_counter_ver2 is
   signal r_reg: unsigned(3 downto 0);
   signal r_next: unsigned(3 downto 0);
begin
   process(mclk,en)
   begin
      if (mclk'event and mclk='1') then
         if (en = '1') then
            if (r_reg = "1001") then
               r_reg <= "0000";
            else
               r_reg <= r_next;
            end if;
         end if;
      end if;
   end process;
   r_next <= r_reg + 1;
   ce_out <= '1' when r_reg = "1001" else '0';
end Behavioral;
```

FPGA Utilization Comparisons

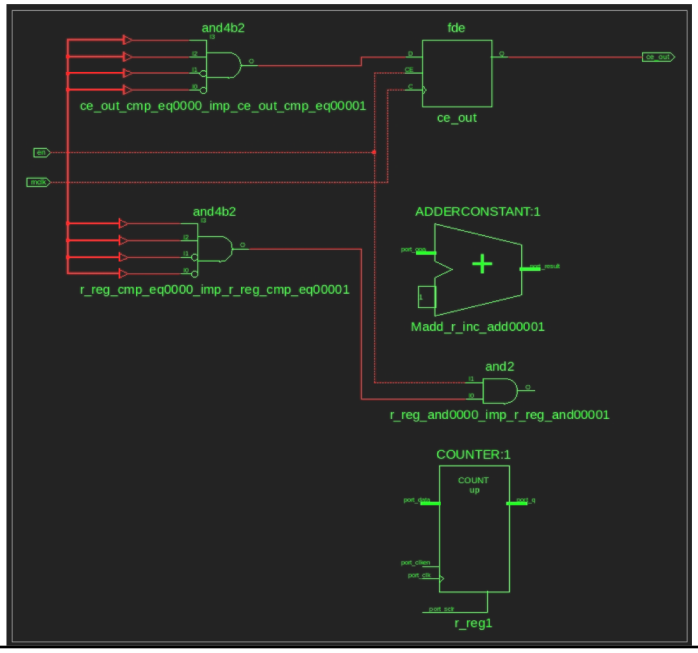
Version 1

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	5	4,896	1%	
Number of 4 input LUTs	5	4,896	1%	
Number of occupied Slices	3	2,448	1%	
Number of Slices containing only related logic	3	3	100%	
Number of Slices containing unrelated logic	0	3	0%	
Total Number of 4 input LUTs	5	4,896	1%	
Number of bonded IOBs	3	66	4%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.25			

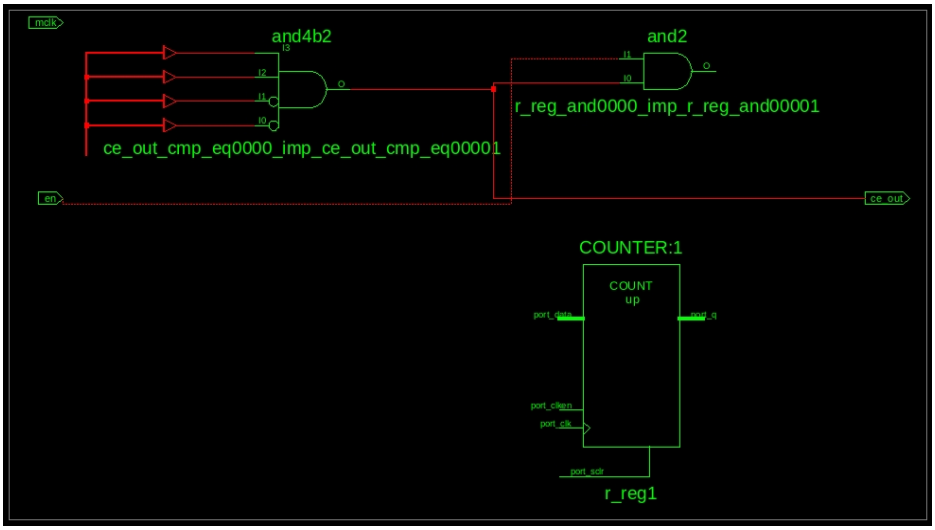
Version 2

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	4	4,896	1%	
Number of 4 input LUTs	5	4,896	1%	
Number of occupied Slices	3	2,448	1%	
Number of Slices containing only related logic	3	3	100%	
Number of Slices containing unrelated logic	0	3	0%	
Total Number of 4 input LUTs	5	4,896	1%	
Number of bonded IOBs	3	66	4%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.57			

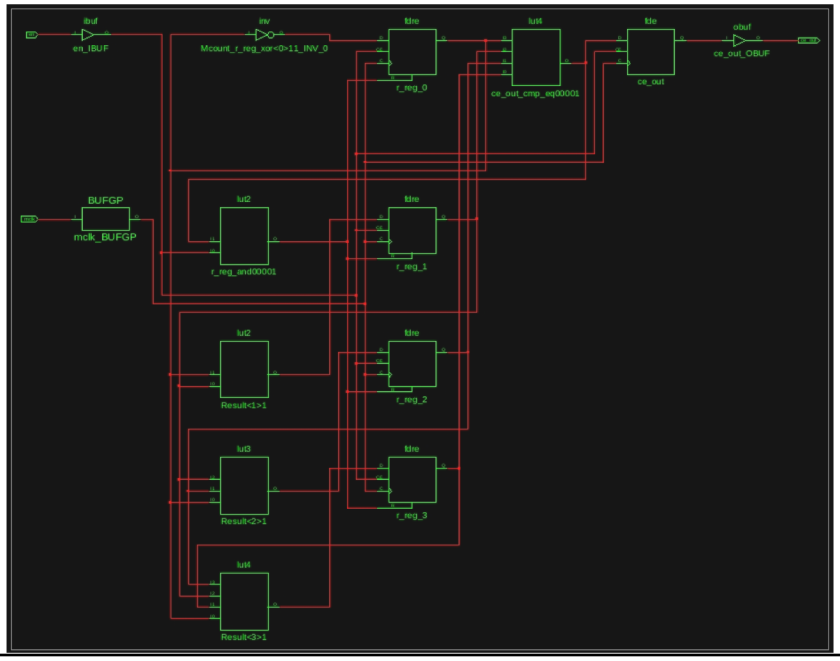
RTL View – Version 1



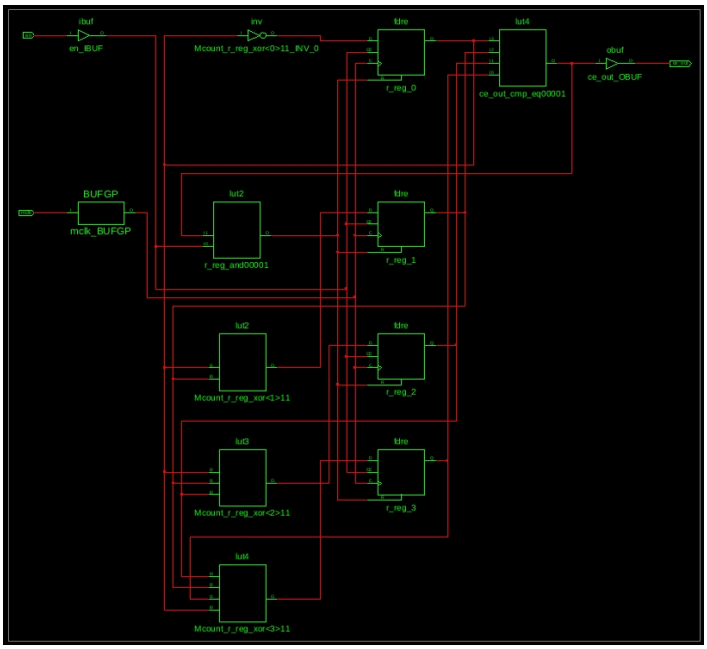
RTL View – Version 2



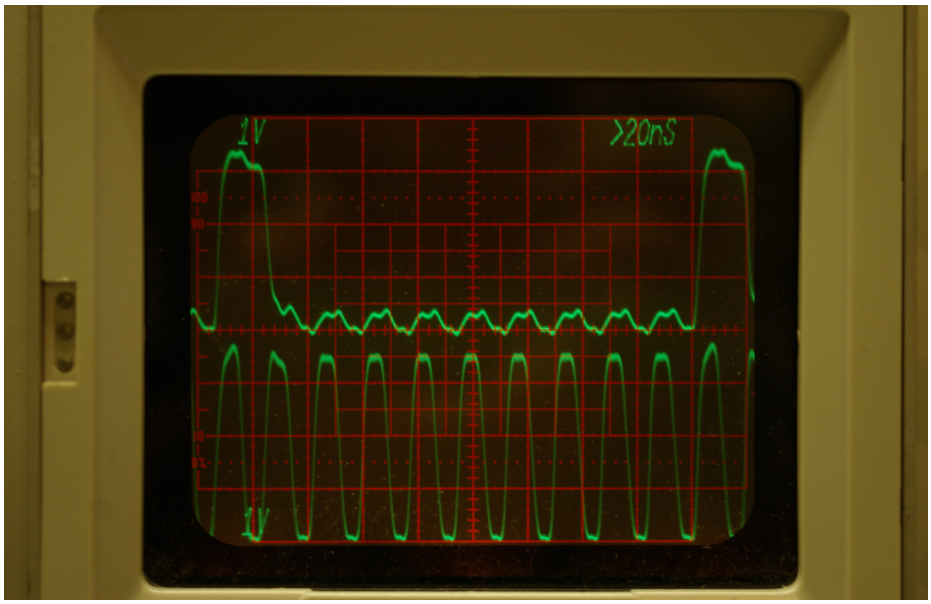
Tech View – Version 1



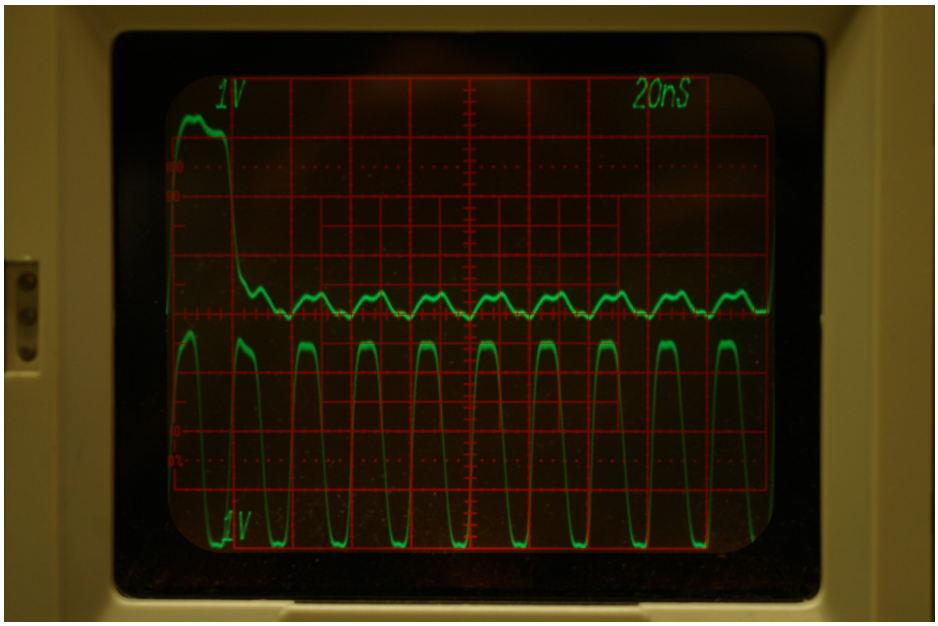
Tech View – Version 2



Timing – Version 1



Timing – Version 2



Behavioral Divide by 1,000,000 - Example 1

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity div_by_1000000_ver1 is
    Port ( mclk : in  STD_LOGIC;
           sclk_out : out  STD_LOGIC;
           mclk_out : out  STD_LOGIC);
end div_by_1000000_ver1;


architecture Behavioral of div_by_1000000_ver1 is
--   divide by 1000000, so 20 bits needed
   signal r_reg: unsigned(19 downto 0);
   signal r_next: unsigned(19 downto 0);
begin
   process(mclk)
   begin
      if (mclk'event and mclk='1') then
         if (r_reg = 999999) then
            r_reg <= (others=>'0');
            sclk_out <= '1';
         else
            r_reg <= r_next;
            sclk_out <= '0';
         end if;
      end if;
   end process;
   r_next <= r_reg + 1;
   mclk_out <= mclk;
end Behavioral;
```

Behavioral Divide by 1,000,000 - Example 2

```
architecture Behavioral of div_by_1000000_ver2 is
--   divide by 1000000, so 20 bits needed
   signal r_reg: unsigned(19 downto 0);
   signal r_next: unsigned(19 downto 0);
begin
   process(mclk,r_reg)
   begin
      if (mclk'event and mclk='1') then
         if (r_reg = 999999) then
            r_reg <= (others=>'0');
         else
            r_reg <= r_next;
         end if;
      end if;
   end process;
   r_next <= r_reg + 1;
   sclk_out <= '1' when r_reg = 999999 else '0';
   mclk_out <= mclk;
end Behavioral;
```

FPGA Utilization Comparisons

Version 1

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	21	4,896	1%	
Number of 4 input LUTs	6	4,896	1%	
Number of occupied Slices	14	2,448	1%	
Number of Slices containing only related logic	14	14	100%	
Number of Slices containing unrelated logic	0	14	0%	
Total Number of 4 input LUTs	25	4,896	1%	
Number used as logic	6			
Number used as a route-thru	19			
Number of bonded IOBs	3	66	4%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.21			

Version 2

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	20	4,896	1%	
Number of 4 input LUTs	6	4,896	1%	
Number of occupied Slices	13	2,448	1%	
Number of Slices containing only related logic	13	13	100%	
Number of Slices containing unrelated logic	0	13	0%	
Total Number of 4 input LUTs	25	4,896	1%	
Number used as logic	6			
Number used as a route-thru	19			
Number of bonded IOBs	3	66	4%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.25			

Structural Divide by 1,000,000 Using Counters

```
entity div_by_1000000_struct is
    Port ( mclk : in  STD_LOGIC;
           mclk_out : out  STD_LOGIC;
           sclk_out : out  STD_LOGIC);
end div_by_1000000_struct;

architecture Behavioral of div_by_1000000_struct is

   component dec_counter
      Port ( mclk : in  STD_LOGIC;
             en : in  STD_LOGIC;
             ce_out : out  STD_LOGIC);
   end component;
   signal ce1,ce2,ce3,ce4,ce5: std_logic;
begin
   u1: dec_counter port map (mclk,'1',ce1);
   u2: dec_counter port map (mclk,ce1,ce2);
   u3: dec_counter port map (mclk,ce2,ce3);
   u4: dec_counter port map (mclk,ce3,ce4);
   u5: dec_counter port map (mclk,ce4,ce5);
   u6: dec_counter port map (mclk,ce5,sclk_out);
   mclk_out <= mclk;
end Behavioral;
```

FPGA Utilization Comparisons

Structural

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	24	4,896	1%	
Number of 4 input LUTs	29	4,896	1%	
Number of occupied Slices	17	2,448	1%	
Number of Slices containing only related logic	17	17	100%	
Number of Slices containing unrelated logic	0	17	0%	
Total Number of 4 input LUTs	29	4,896	1%	
Number of bonded IOBs	3	66	4%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.97			

Behavioral – Ver 2

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	20	4,896	1%	
Number of 4 input LUTs	6	4,896	1%	
Number of occupied Slices	13	2,448	1%	
Number of Slices containing only related logic	13	13	100%	
Number of Slices containing unrelated logic	0	13	0%	
Total Number of 4 input LUTs	25	4,896	1%	
Number used as logic	6			
Number used as a route-thru	19			
Number of bonded IOBs	3	66	4%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.25			

Testing r_next Instead of r_reg Comparison

```
architecture Behavioral of div_by_1000000_ver2 is
--   divide by 1000000, so 20 bits needed
   signal r_reg: unsigned(19 downto 0);
   signal r_next: unsigned(19 downto 0);
begin
   process(mclk,r_reg)
   begin
      if (mclk'event and mclk='1') then
         if (r_reg = 999999) then
            r_reg <= (others=>'0');
         else
            r_reg <= r_next;
         end if;
      end if;
   end process;
   r_next <= r_reg + 1;
   sclk_out <= '1' when r_reg = 999999 else '0';
   mclk_out <= mclk;
end Behavioral;
```

```
architecture Behavioral of div_by_1000000_ver4 is
--   divide by 1000000, so 20 bits needed
   signal r_reg: unsigned(19 downto 0);
   signal r_next: unsigned(19 downto 0);
begin
   process(mclk,r_next)
   begin
      if (mclk'event and mclk='1') then
         if (r_next = 1000000) then
            r_reg <= (others=>'0');
         else
            r_reg <= r_next;
         end if;
      end if;
   end process;
   r_next <= r_reg + 1;
   sclk_out <= '1' when r_next = 1000000 else '0';
   mclk_out <= mclk;
end Behavioral;
```

FPGA Utilization Comparisons

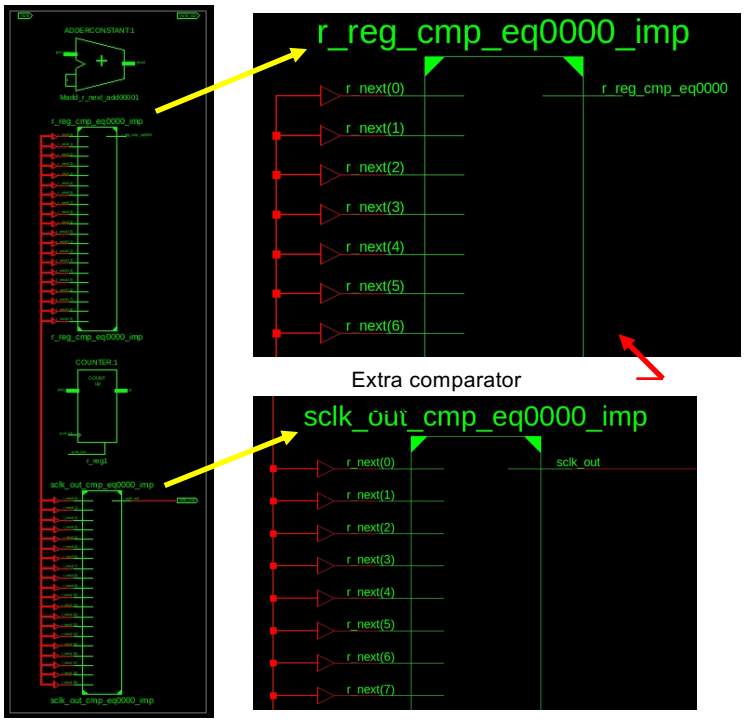
Version 2

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	20	4,896	1%	
Number of 4 input LUTs	6	4,896	1%	
Number of occupied Slices	13	2,448	1%	
Number of Slices containing only related logic	13	13	100%	
Number of Slices containing unrelated logic	0	13	0%	
Total Number of 4 input LUTs	25	4,896	1%	
Number used as logic	6			
Number used as a route-thru	19			
Number of bonded IOBs	3	66	4%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.25			

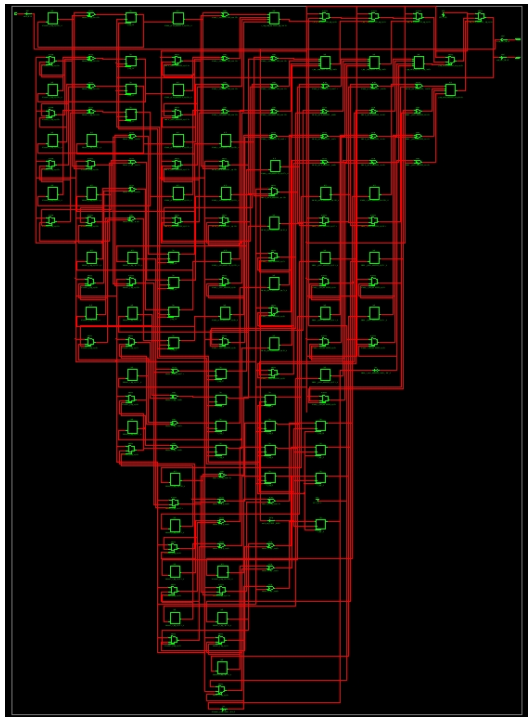
Version 4

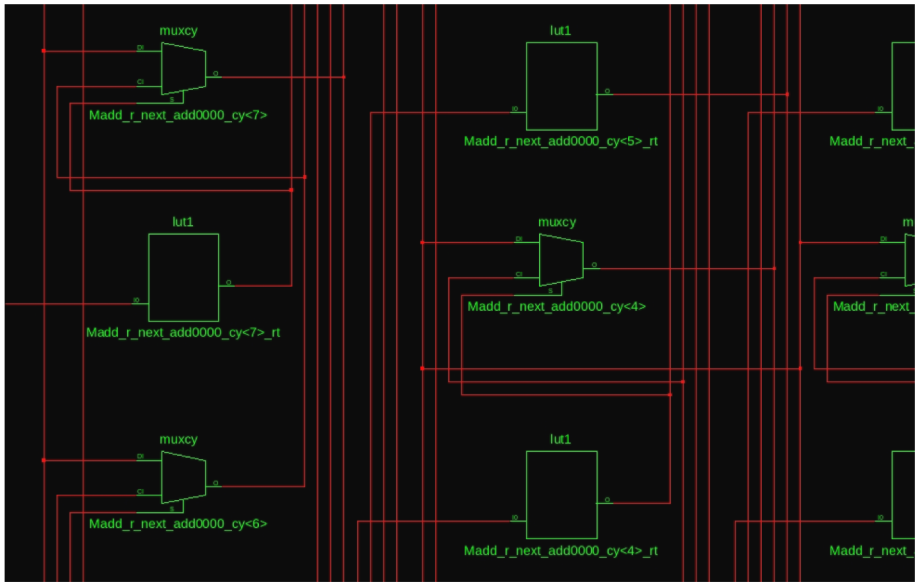
Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	20	4,896	1%	
Number of 4 input LUTs	7	4,896	1%	
Number of occupied Slices	23	2,448	1%	
Number of Slices containing only related logic	23	23	100%	
Number of Slices containing unrelated logic	0	23	0%	
Total Number of 4 input LUTs	45	4,896	1%	
Number used as logic	7			
Number used as a route-thru	38			
Number of bonded IOBs	3	66	4%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	1.66			

RTL view ver4



Tech view ver4





Tech view, ver4 (zoomed in)